IN THE SPECIFICATION:

Please revise the specification as follows:

Please amend paragraph 0034:

FIG. 4 is a block diagram of a demultiplexer in a preferred embodiment of the error counter of the present invention. Demultiplexer 402 receives error flag data from a ~~multplexed~~ multiplexed stream on bus 404. Demultiplexer 402 is able to identify error flag data in response to an error clock signal (Clk E) on line ~~404~~ 406. Although many schemes exist, the present invention makes use of error flag bits 7 through 11 (*i.e.*, Eflg11:7) in an error stream (*i.e.*, Eflg23:0) as shown in the table above. Error flag bits 7 through 11 are used by C1 and C2 error detection and correction schemes where bits 10 and 11, identified as Eflg10 and Eflg11 respectively, are used for C1 error detection and bits 7 through 9 are used for C2 error detection, identified as Eflg7 through Eflg9 (see table above). In a particular embodiment of the preferred invention, Eflg11:7 are output in parallel form. That is to say, a large serially multiplexed stream of data is input into demultiplexer 402 and the same information is output in parallel form. It will be obvious to one skilled in the art to implement demultiplexer 402 in other forms. For example demultiplexer 402 may be implemented to filter only the error flag bits of interest. In this way, error flag bits Eflg11:7 can be output in a shortened multiplexed form and then processed as will be further described below.

Please amend paragraph 0035:

Referring now to FIG. 5, the demultiplexed error data (*i.e.*, Eflg11:7) on bus 408 is fed into decoder 502. Decoder 502 may be implemented in various forms. For example, in one embodiment, decoder 502 may be implement to detect C1 and C2 errors individually. In the embodiment shown in FIG. 5, decoder 502 detects and counts the number of errors within C1 and C2, respectively or collectively. As shown in FIG. 5, write data selector 504 receives signals from the microprocessor 112 (see FIG. 1) in the form of microprocessor input data on line 506 and from read data selector 508. Such signals are accepted by the data selector 504 upon the occurrence of a microprocessor write strobe on line 510. Data selector decoder signal on line 512 is then sent to the counter control register 514. In turn, counter control register 514 sends an appropriate signal (*i.e.*, C1unc) on line 516 to decoder 502 to process particular types of C1 errors. For example, the signal on line 516 may designate that counting should be done when the C1 frame contains 1 error. Alternatively, the same could be done when the C1 frame contains 2 errors or is uncorrectable. Furthermore, counter

control register 514 sends an appropriate signal (i.e., C2unc) on line 518 to decoder 502 to process particular types of C2 errors. In this manner, the microprocessor 112 controls the type of errors, either C1 and/or C2, as well as the numbers of errors within each error type that decoder 502 will process.

Please amend paragraph 0044:

The error rate counter of the present invention has as a preliminary stage a demultiplexer as shown in FIG.4. The operation of demultiplexer 402 is as described above. Referring now to FIG. 7, the demultiplexed error data ~~404~~ 408 (*i.e.*, Eflg11:7) is then fed into decoder 502. Decoder 502 may be implemented in various forms as previously described for FIG. 5. Upon the occurrence of C1 errors of an identified type, an appropriate C1 count-up signal on line 520 is sent to C1 error per second (EPS) counter 702. Similarly, a C2 count-up signal on line 524 is applied to the C2 error per second counter (EPS) 704. C1 EPS counter 702 and C2 EPS counter 704 increment on the occurrence of frame clock signal on line ~~528~~ 706.